EAST - [default 1.wsp:1]

File View Edit Tools Window Help

- Active
  - L1: (8010) synchronous adj4 memory
  - L2: (732948) latch or register
  - L3: (722590) counter
  - L4: (2336) data adj2 strobe adj2 signal
  - L5: (680518) clock$4
  - L6: (108534) 2 same 3
  - L7: (173) 4 same 6
  - L8: (87) 5 same 7
  - L10: (18) 1 and 8
  - L11: (69) 8 not 10
  - L12: (86) 7 not 8
  - L25: (4382) 365/189.05
  - L27: (2084) 365/194
  - L28: (4428) 365/233
  - L29: (897) 365/236
  - L30: (638) 365/219
  - L31: (360) (data adj2 strobe) same 6
  - L33: (0) 31 and 26
  - L35: (29) 31 and 28
  - L37: (0) 31 and 30
  - L32: (20) 31 and 25
  - L38: (12) 35 not 32
  - L34: (12) 31 and 27
  - L36: (4) 31 and 29
  - L39: (194254) 365/
  - L40: (72) 31 and 39
  - L41: (43) 40 not 35
  - L42: (40) 41 not 32
- Failed
- Saved

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DBs: USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB — Plurals

Default operator: OR — Highlight all hit terms initially

BRS form | ISR form | Image | Text | HTML

| | U | 1 | 2 | Document ID | Issue Date | Pages | Title | Current OR | Current XRef | Retrieval Cla | Inventor | S | C | F |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 1 | | ☑ | | US 6115322 A | 20000905 | 44 | Semiconductor device accepting data which includes serial data signals, in synchronization with a | 365/233 | 365/189.05; 365/230.08 | | Kanda, Tatsuya et al. | ☑ | | |
| 2 | | ☑ | | US 6147926 A | 20001114 | 16 | Semiconductor memory device | 365/233 | 365/189.05; 365/221; 365/236 | | Park, Boo Yong | ☑ | | |
| 3 | | ☑ | | US 6324119 B1 | 20011127 | 19 | Data input circuit of semiconductor memory device | 365/233 | 365/222 | | Kim, Chi-wook | ☑ | | |
| 4 | | ☑ | | US 6407963 B1 | 20020618 | 19 | Semiconductor memory device of DDR configuration having improvement in glitch immunity | 365/233.5 | 365/233 | | Sonoda, Takahiro et al. | ☑ | | |

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NUM

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